

CONTINUOUS PROCESS IMPROVEMENT

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SUMMARY

The Electronic Fabrication Section at the Jet Propulsion Laboratories (JPL) has been studying ways to improve Printed Wiring Assembly (PWA) processes.

The PWA study described here contained typical surface mount devices including 20 mil fine pitch devices and various BGAs.

All the processes, beginning from design for manufacturability through rework/repair, were studied. JPL assembles low-volume, high-reliability products for ground and space applications presenting unique manufacturing challenges. Some of the processes and the challenges are described in this paper.

Figure 1 depicts a typical assembly flow at JPL. Processes details are described in the subsequent paragraphs.

1. Design for Manufacturability

To achieve maximum process yield, it is important to design a board considering the following factors:

Surface mount component footprint design

IPC-SM-782x specification has good guidelines for proper footprint design, however, there are unique components, such as MELF and flat packs, that require detailed package evaluation. If the pads are too small, the result can be insufficient solder. If they are too large, the result may be tombstoning or components shifting off the pads. (see Figure 2).

Pad design for 20 mil pitch QFP must have a minimum 10 mil to maximum 35 mil long pad on toe and heel side of a lead. Desirable pad width is between 9 and 11 mil. BGA pad design will depend on BGA ball size and ball pitch. A typical BGA package had 30 mil diameter balls at 50 mil pitch. For this configuration, the pad size was designed to be 26 mil. Each of the BGA pads were connected to a nearby plated through hole by a short trace forming a 'dogbone' structure. If multiple BGAs are used, they should be distributed as evenly as possible throughout the board to balance the thermal load.

To increase the solder joint reliability it is best to apply solder mask on the periphery of the BGA pads. This is to provide a high standoff between the board surface and the package after reflow. A 0.2 inch clearance around the IC should be allowed for rework nozzle in case the BGA needs removal and replacement.

Components must be evenly distributed throughout the board, and, use of localized large 'ground' plane must be avoided. If this is not done, uneven heating of the board may result in warpage and unreliable solder joints.

2. Component Lead Forming

Flat packs are widely used in military and aerospace manufacturing environments. Flat pack vendors generally do not preform flat packs since the footprint design may vary from one user to another. Hence most flatpacks and some QFPs require preforming of the leads.

Use of proper forming dies is critical to form the parts with burr free leads. Die design was based on footprint specification set forth during the design stage.

3. Lead tinning (solder coating)

For reliable solder joint formation it is essential that the IC leads are corrosion free and readily solderable. Gold-plated leads must be free of gold and coated with solder to eliminate formation of gold tin **intermetallics**, which can cause cracks in solder joints due to a phenomenon known as gold-tin **embrittlement**.

At JPL, all IC'S are tinned using robotic tinning equipment with nitrogen inerted dual solder pots. The entire process is described in a flowchart shown in Figure 3. Equipment and processes are computer controlled.

4. Coplanarity Check

After tinning, all IC leads are checked for coplanarity. For space flight applications, leads must be coplanar within .004 inch. Using a laser-based instrument, lead coplanarity is checked and corrected as required before assembly.

5. Printed Wiring Board Testing

Two types of tests are performed on JPL boards:

- electrical
- solderability

Electrical test:

The purpose of this test is:

- To ensure there are no opens or shorts on the board
- To verify the CAD file against the fabricated board

The equipment has dual programmable probes that contact each 'net' at high speed and check for open and shorts. Test results are printed at the end of the test. One sample board from each lot is tested.

Solderability Test

To form a high-reliability solder joint, it is essential that the pads and holes on the PWB surface are contaminant free. Contaminants are mostly copper and tin oxides which, if not cleaned, can cause solderability problems. A solderability tester operating on the principle of Sequential [Electro-chemical Reduction Analysis (SEIRA)] is used to measure PWB solderability. The SEIRA method involves a chemical reduction of metal oxides by applying an electrolyte on the PWB surface. The electrolyte solution consists of sodium

borate and boric acid solution with a PH of 8.4. As the electrolyte reacts with oxides, voltage is measured. Depending on the type and the amount of oxide, a curve is created (Figure 4).

As shown in this curve, copper and lead oxides are easily removed with flux applied before soldering. Lower tin oxide (such as SnO) can be reduced by the flux. Hence, voltage levels of -1 (negative one) volt and above are acceptable. However, if the negative voltage reached below -1 volt, the board may have higher tin oxides and is therefore rejected due to the difficulty in soldering the surface.

Figure 5 shows a chart for a board that failed the solderability test. Figure 6 shows a similar chart for a board that passed the test.

6. Kitting

Following the preparation of all board components they are transferred to the kitting area to be kitted according to package types and whether or not they are assembled prior to reflow or after reflow.

7. Screen Printing

Before screen **printing**, boards are cleaned in an aqueous cleaner using DI water and saponifier solution followed by an alcohol rinse to insure that the board surface is contaminants free. Next the boards are vacuum baked @ 100° C for 8 hours to ensure that moisture is removed.

The stencil printer is fitted with:

- Tooling plate with double-sided board screening capability
- Fine adjustment micrometers for accurate registration between stencil apertures & PWB pads
- Programmable squeegee pressure
- Vacuum-assisted board holding for warped boards
- Different viscosity pastes and various stencils apertures
- For high reliability space applications, only Sn63 paste with RMA flux is approved for use

After a series of trials the following parameters were found to produce optimum printing:

Stencil thickness of 7 mil

Paste viscosity 1000 KCPS \pm 200 kcps

Paste mesh size of -325/+500

Squeegee pressure of 10 lb. For 7" long metal squeegee

Stencil aperture size reduced to approx. 85% of the size of the pad (see Figure 7 for BGA pad)

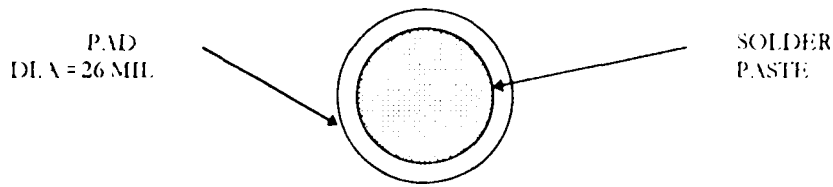


Figure: 7

Figures 8 & 9 show typical prints of the solder paste prints for a BGA configuration. The height of the solder paste at several locations was measured using laser-based measurement systems. As shown in Figure 10, the height variation was within plus or minus 2 mils. Also, Figures 11 & 12 show graphically the variation of solder paste height.

8. Pick and place of components

Components are available/arrive in various types of packaging styles such as:

- Tape and reel
- Strips of tape
- In waffle packs and matrix trays
- In tubes
- Loose

In a low-volume environment, feeding components to pick and place machines offers numerous challenges. The major issues are:

- components are generally not provided on tape and reel
- there is limited real estate on a machine table to accommodate various types of stripped parts and waffle/matrix trays.

Loose parts can be sent out for taping and reeling, however, it may not be practical to do so in all cases. For example, if the quantity of components is very small, it may not be cost effective to tape and reel; also in some instances, lead time for taping and reeling from outside services may be prohibitively longer.

At JPL, parts are received in various packaging styles. Most discrete components are in strips of tape or waffle packs. Some IC's are received loose and some in tubes. To accommodate most part numbers from a kit on the pick and place machine and to avoid frequent changeovers, we designed our own feeder system. Since the machine was capable of picking up parts from anywhere within the X-Y table (including those in taped strips and waffle packs), the feeder system was designed to be flexible and efficient for low volume production application.

Figures 13, 14 and 15 show examples of various feeders currently in use. The trays shown in Figure 13 are chosen for placing strips of tape. Tray design is such that it can be interchangeable with the fixture used for the robotics tinning machine for parts pick up. Small IC's are placed in either vibratory feeders or waffle trays. Fine pitch QFP's and BGAs are placed in matrix trays as shown in Figures 14 and 15.

A set up sheet is prepared for each assembly type, enabling an operator to set up the machine with various parts at their proper location (see Figure 16).

Y-axis/matrix tray dimensions, strip tape dimensions and location of first and diagonally opposite (last) components are stored in the machine library. Once this is accomplished, the trays or strips can be placed anywhere on the X-Y table. The machine only needs to be programmed for the two corners of the first and last components for accurate pick up.

Pick and place equipment has the following capabilities:

- Automatic fiducial check and correction
- Automatic package size verification
- Automatic electrical value verification for resistors, capacitors & diodes
- Coplanarity check for fine pitch parts
- BGA vision check
- Smart Feeder
- Automatic "Z" height adjustment

For parts with oversized pad design, it is critical that the part centroid and the pad centroid are within 5 mil of each other. If not, it may shift off the pad or tombstone during reflow.

9. Reflow

Prior to soldering a PWA, a reflow profile is created using a multi-channel, microprocessor-based temperature recording instrument. For BGA parts, the thermocouples are placed under the device by drilling a hole on PWB (see Figure 17). After a series of trials, a final profile is obtained (Figure 18).

Computer controlled vapor phase reflow equipment is used for solder paste reflow of the PWA. The entire reflow cycle is described in a flowchart (Figure 19).

10. Rework

Computer-controlled hot gas reflow equipment is used for removing and replacing components on the PWB. The equipment is built with the following capabilities:

- Split mirror vision allowing simultaneous viewing of component leads and PWB pads for accurate registration
- Infrared pyrometer for real-time temperature measurement
- Three channels of thermocouples for temperature profiling
- Bottom side preheater
- Closed loop temperature feedback for nozzle temp & bottom preheater temp.
- Control mechanism for controlling rate of gas flow
- All parameters such as temp, duration and flow rate can be entered, edited and stored in a computer

Component Removal Operation

It is extremely important that heat be applied in a similar manner as used during PWA reflow operations. The PWA must be heated gradually at the rate of 2-4° C per second, creating a thermal profile. If there are components close to the one to be removed, those components may be masked with a high temp. tape or other similar means. This is to prevent the solder joints at those locations from melting due to heat migration during rework.

It is equally important to preheat the board from the bottom side, thereby reducing thermal shock. The profiles for several components were generated using actual scrapped parts. An infrared pyrometer was attached to monitor the top-side temperature of one of the IC leads. In the case of BGA, a pyrometer was used to measure the temperature of the top side of the package and a thermocouple was inserted and glued on a pad, under the device from bottom side, by drilling hole. Heat application time was maintained between 50 and 120 seconds during the liquid state.

Figures 20 to 22 show profiles for the above-mentioned components.

Special precautions for Plastic BGAs

The profile for Plastic BGAs requires more gradual heating of the part (under 2° C per second). This is due to the fact that Plastic BGAs have molding compound over the die surface, resulting in a thicker package at the center compared to the thinner outer periphery. If heated at a faster rate, it may warp at the outer periphery causing solder bridges.

Component Placement and Soldering Operation

The component placement and soldering operation is more critical and demands a higher degree of process control in order to form reliable solder joints.

Prior to the placement of new components, the board surface is prepared as follows:

- clean board surface of any flux residue and excess solder
- apply solder to the pads.

The solder may be applied by:

- adding solder with core solder and soldering on
- dispensing solder paste on pads
- screening solder paste on pads

The method may vary according to the type of component to be soldered and equipment availability. For fine-pitch components, any of the above methods are suitable. However, for fine pitch and BGA components, it is best to use solder paste. Since the pads of these components are smaller and are spaced less than 25 mil pitch, the proper amount of paste deposition is critical. Solder paste will perform a dual function of forming a solder joint and

holding the component at its proper location during solder reflow. In a typical screening method, a mini stencil is used to selectively apply solder paste (Figure 23).

Some of the control parameters affecting the reflow soldering of the components are:

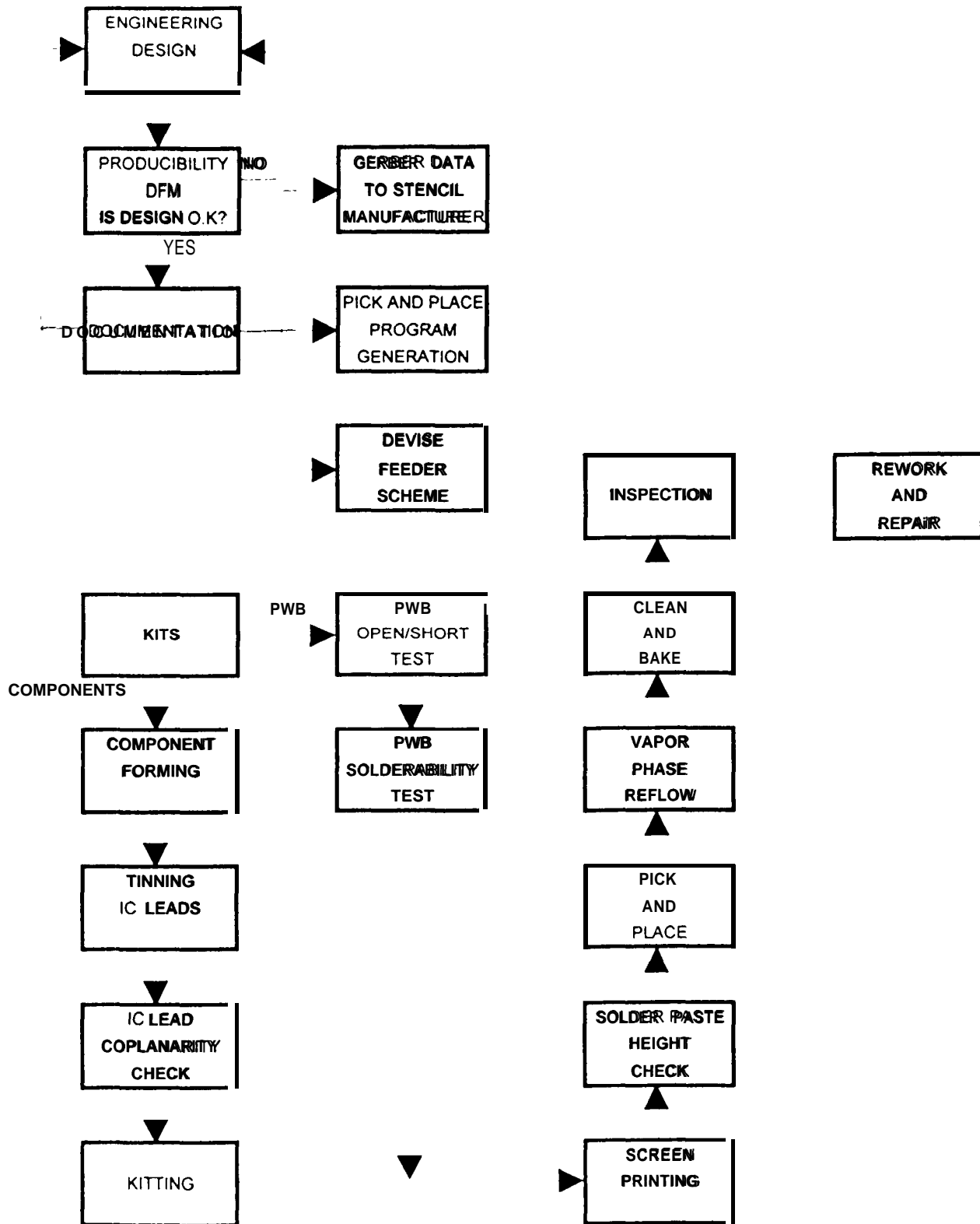
- Amount of solder
- Gas flow rate
- Gas temperature
- Heat application duration

All the above parameters must be properly controlled to achieve reliable solder joints.

For **fine** pitch components such as QFP, it is important that leads are coplanar within ± 0.01 mil.

It is important to note that once Ball Grid Array components are removed, they are not reusable unless they are 're-balled'.

CONTINUOUS PROCESS IMPROVEMENT



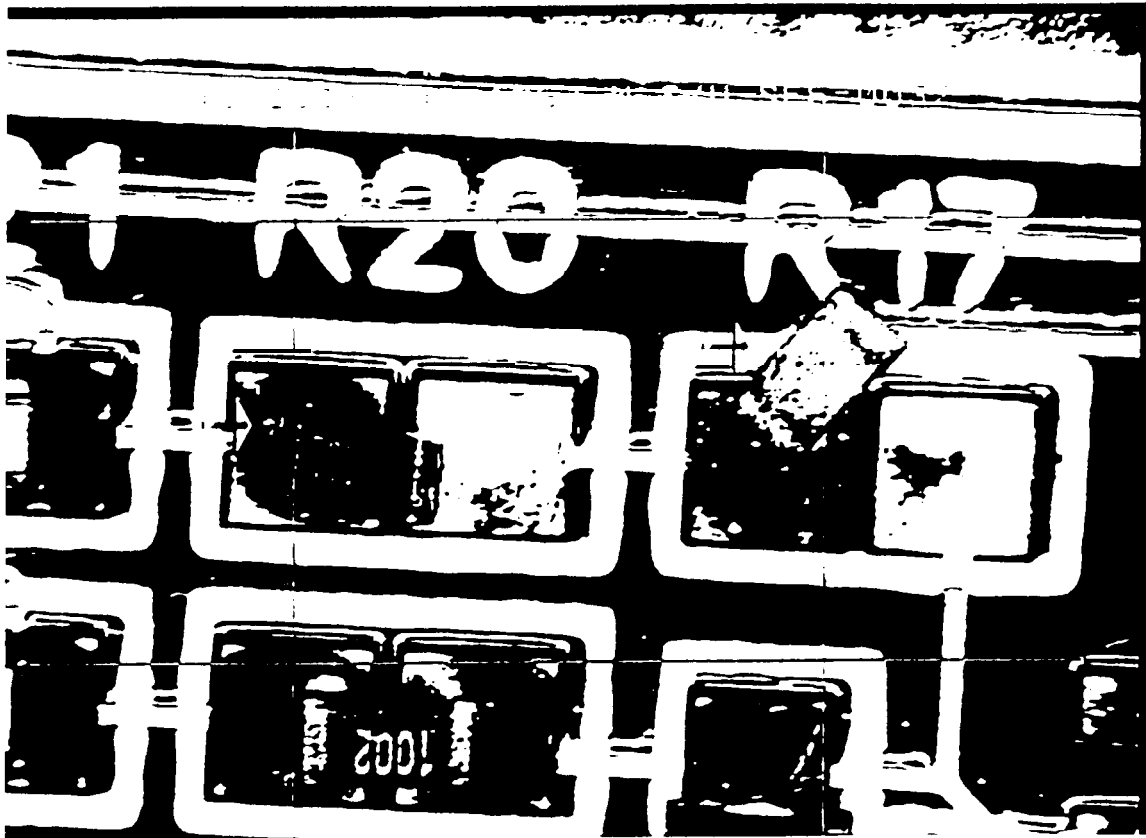


Figure: 2

TINNING OPREATION PROCESS FLOW

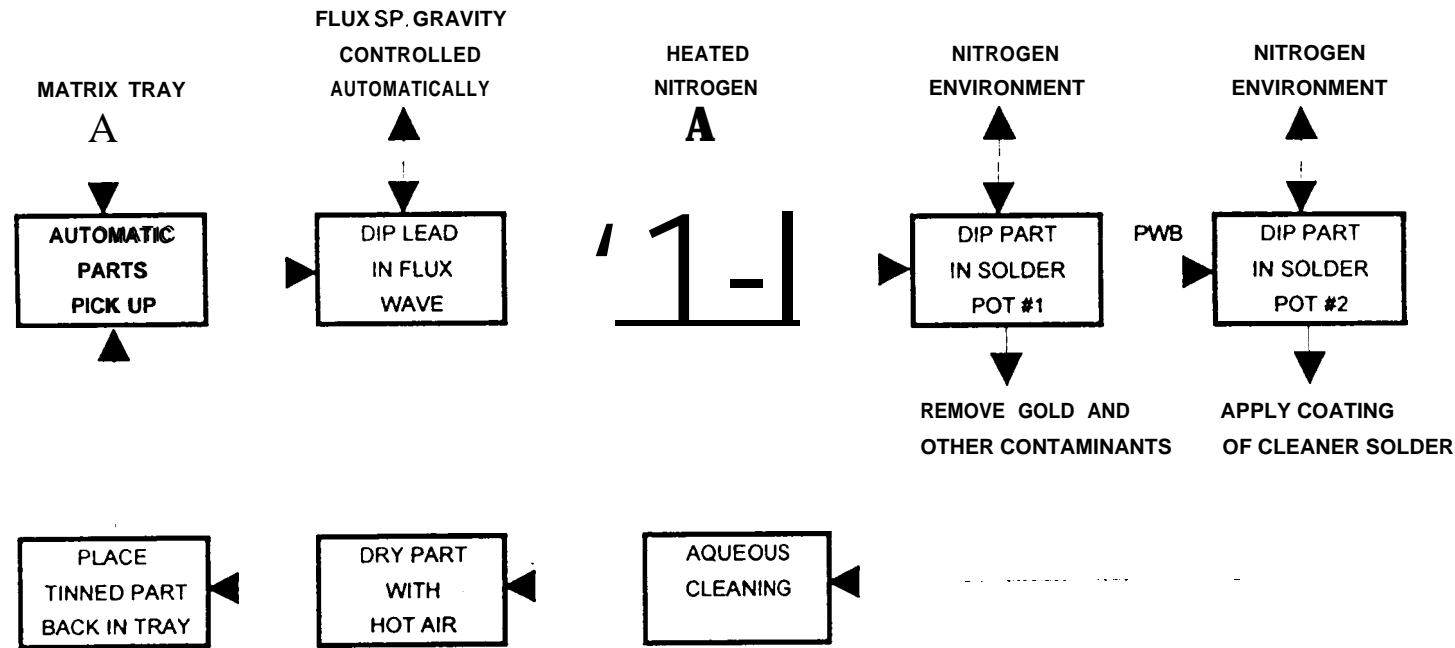


FIGURE 3

SUMMARY OF TEST SIGNALS

VOLTAGE	FEATURE	TYPE OF OXIDE	COMMENTS
-0.35	FLAT PLATEAU	LOWER COPPER OXIDE (CuO)	BOARD ACCEPTABLE "
-0.50	FLAT PLATEAU	LEAD (HYDRATED PbO)	BOARD ACCEPTABLE "
-0.55 To -0.85	BROAD SHOULDER	Cu-Sn INTERMETALLIC	BOARD ACCEPTABLE •
-0.60	FLAT PLATEAU	HIGHER COPPER OXIDE (Cu ₂ O)	BOARD ACCEPTABLE "
-0.60	FIAT PLATEAU	LEAD OXIDE (PbO)	BOARD ACCEPTABLE •
-0.85 To -1.00	FLAT PLATEAU	LOWER TIN OXIDE (MOSTLY SnO)	BOARD REJECTABLE **
-1.00 To -1.30	PLATEAU	MIXTURE OF LOWER AND HIGHER TIN OXIDES (MORE SnO ₂)	BOARD REJECTABLE *
-1.00 To -1.30	NEGATIVE VOLTAGE DIP	HIGHER TIN OXIDE (MOSTLY SnO ₂)	BOARD REJECTABLE ***

* COMMONLY USED FLUXES ARE CAPABLE OF CLEANING THE OXIDES. USE AS IS.

** COMMONLY USED FLUXES MAY NOT CAPABLE OF CLEANING THE OXIDES. IT IS DESIRABLE TO TO PRECLEAN THE PWB PRIOR TO ITS USE.

***PWB MAYBE DIFFICULT TO PRECLEAN AND MAY NOT BE USABLE IN ITS CURRENT STATE.

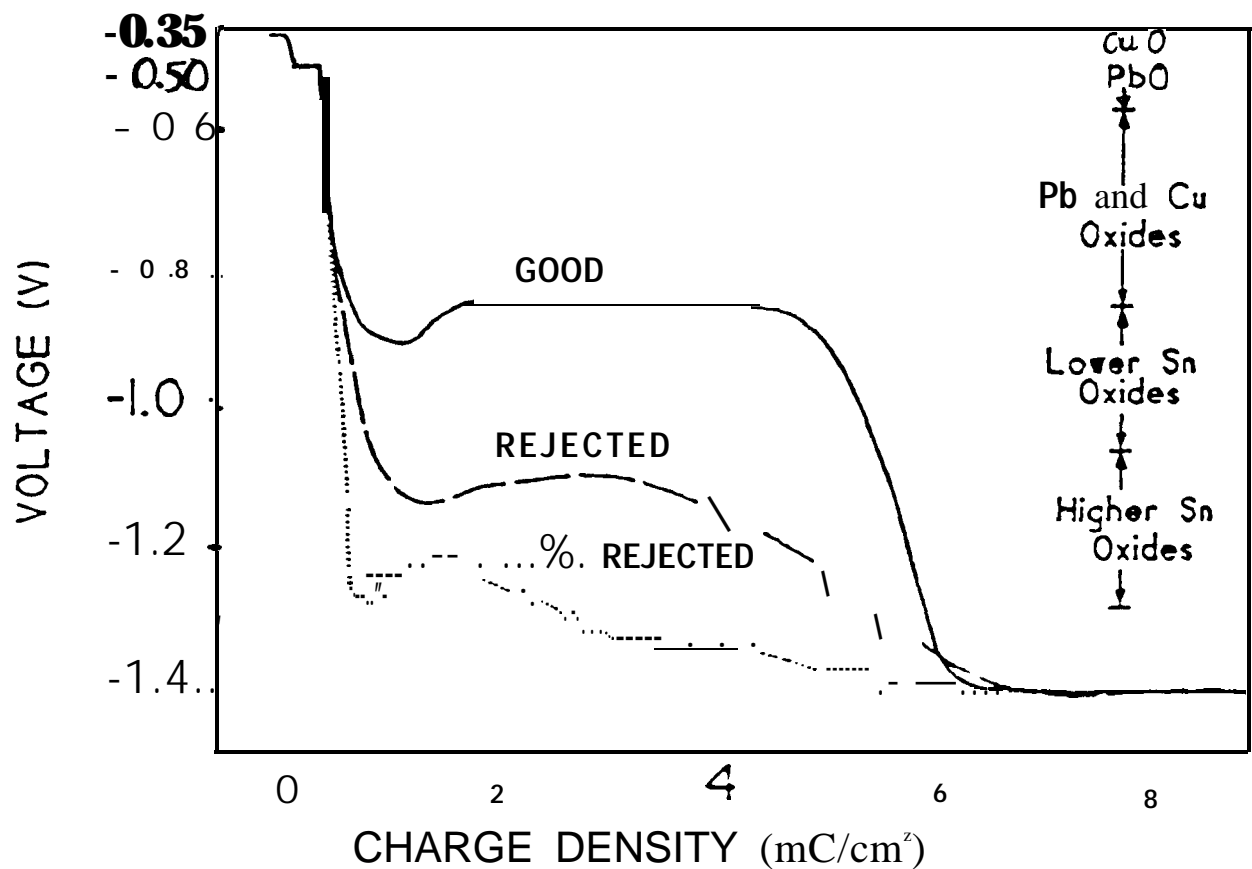


Figure: 4

Part Number: 610112-i

Test Point: 1

Test Comments:

Data file:

\CALTECH\095600.321

Current=0.603 μ A (30.0 μ A/cm²)

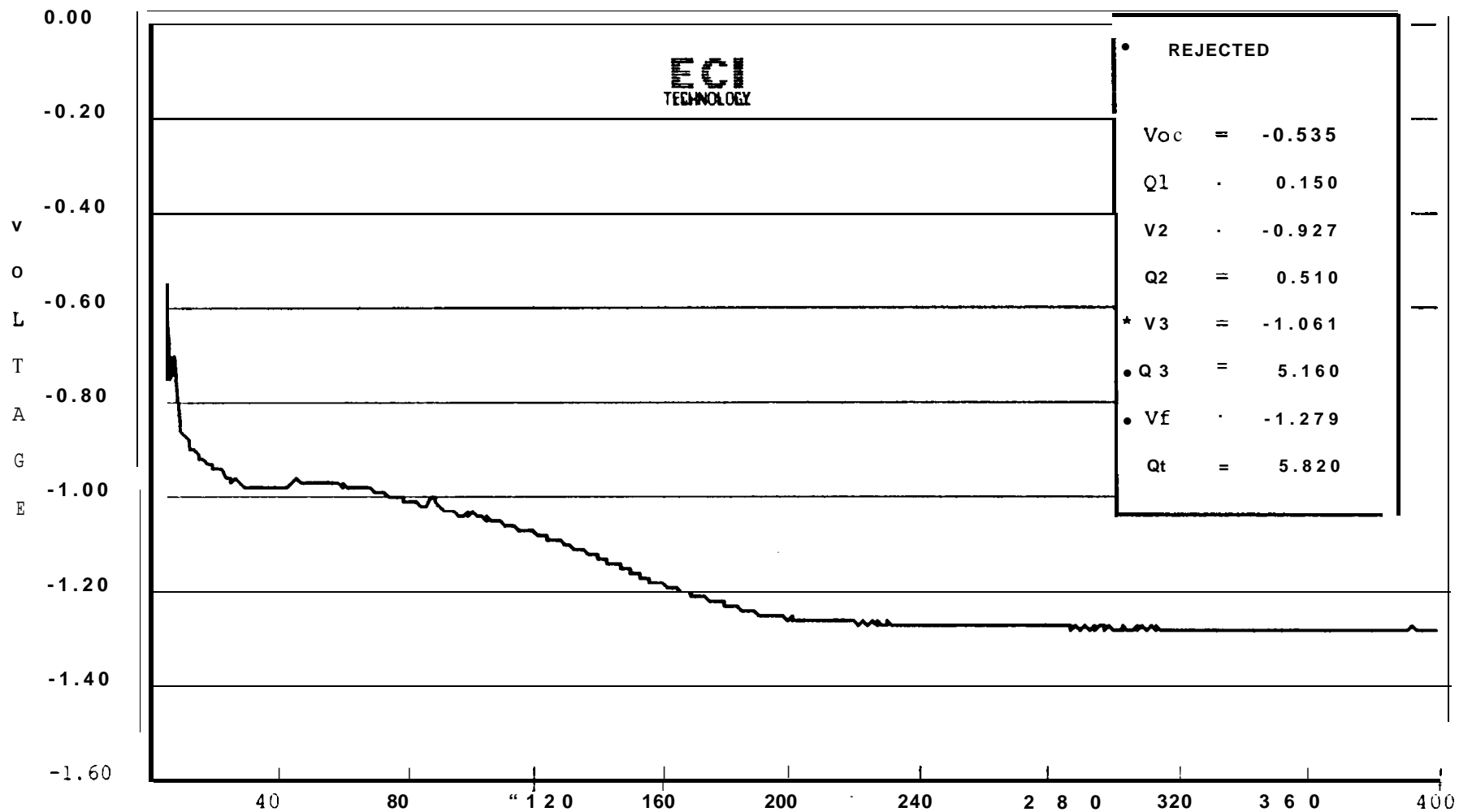


Figure: 5

Part Number: 10150073
Test Point: 1
Test Comments: SMT TEST BOARD

Data file:
\\CALTECH\\105333.321
Current=0.603μA (30.0μA/cm²)

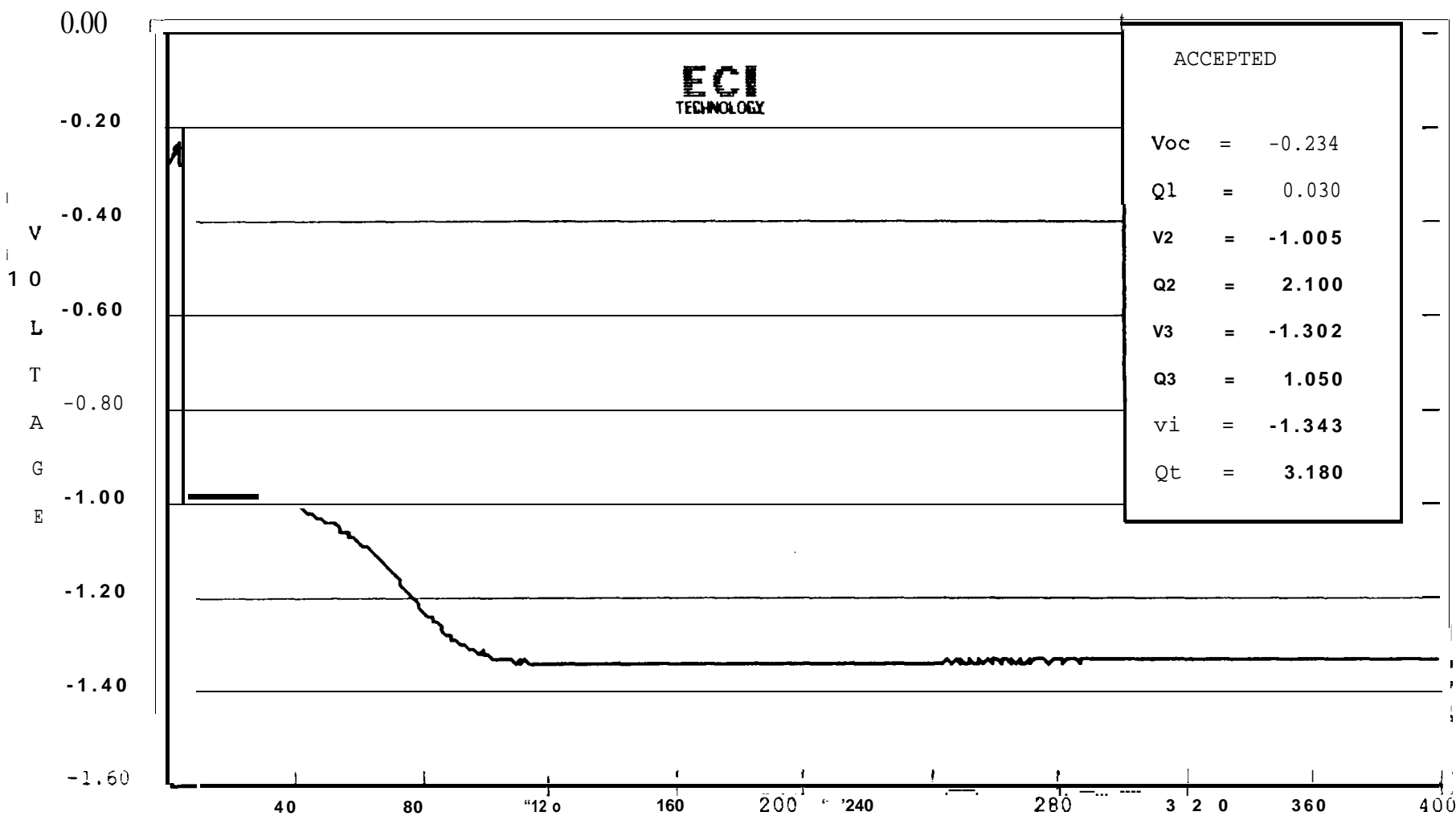


Figure: 6

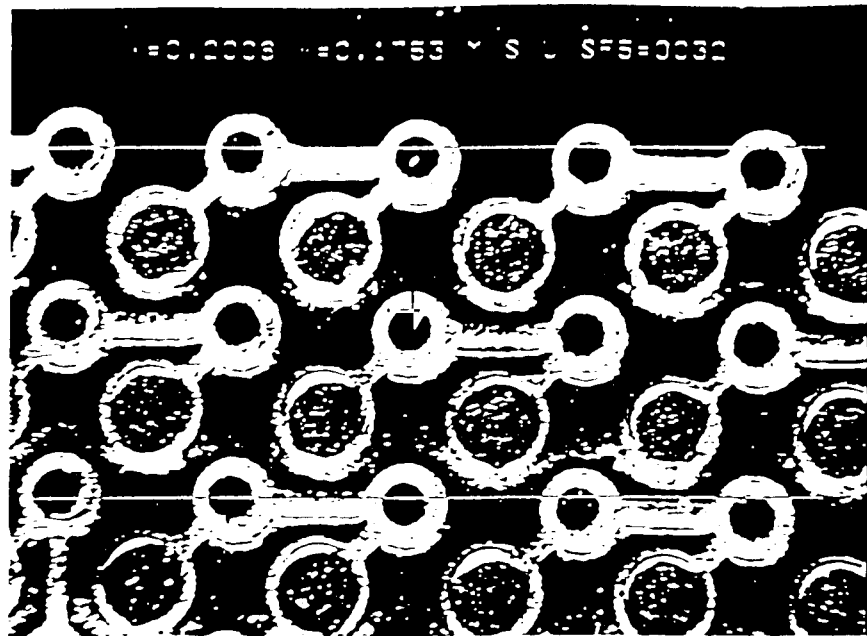


Figure: 8

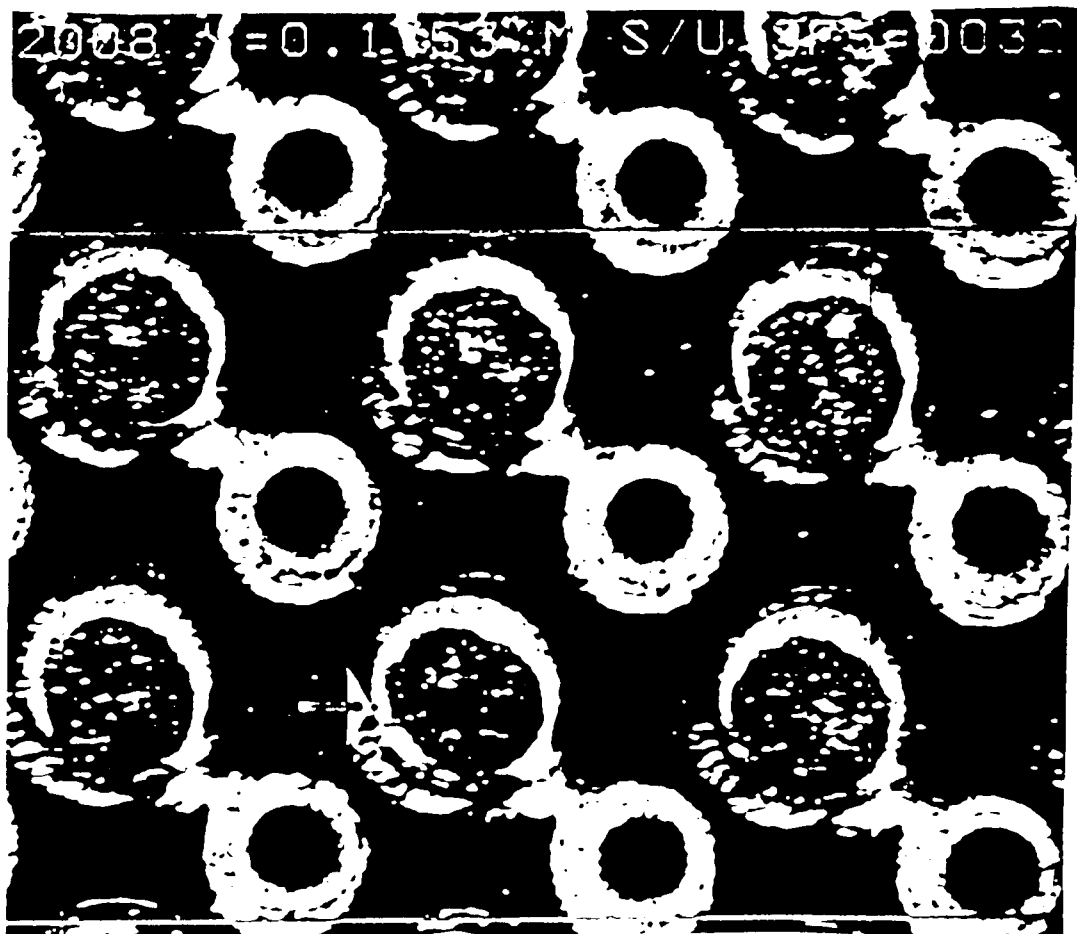


Figure 9

SOLDER, 0.050 PITCH, .		
Time & Date	VOLUME(W)	VOLUME(H)
1 10/24/97 1:55:30 PM	37.9	7.6
2 10/24/97 1:29:30 PM	37.9	7.2
3 10/24/97 1:29:51 PM	37.9	7.6
4 10/24/97 1:30:17 PM	37.9	6
5 10/24/97 1:30:34 PM	37.9	7
6 10/24/97 1:30:55 PM	37.9	7.1
7 10/24/97 1:31:21 PM	37.9	8.5
8 10/24/97 1:32:15 PM	37.9	7.8
9 10/24/97 1:35:44 PM	37.9	7.6
10 10/24/97 1:36:59 PM	37.9	7
11 10/24/97 1:37:35 PM	37.9	7.2
12 10/24/97 1:53:26 PM	37.9	7.6
13 10/24/97 1:54:03 PM	37.9	7.8
14 10/24/97 1:54:39 PM	37.9	7.7
15 10/24/97 1:54:57 PM	37.9	7.3
16 10/24/97 1:55:49 PM	37.9	7.8
17 10/24/97 1:56:09 PM	37.9	7.4
18 10/24/97 1:56:21 PM	37.9	7.5
19 10/24/97 1:56:42 PM	37.9	7.1

Figure: 10

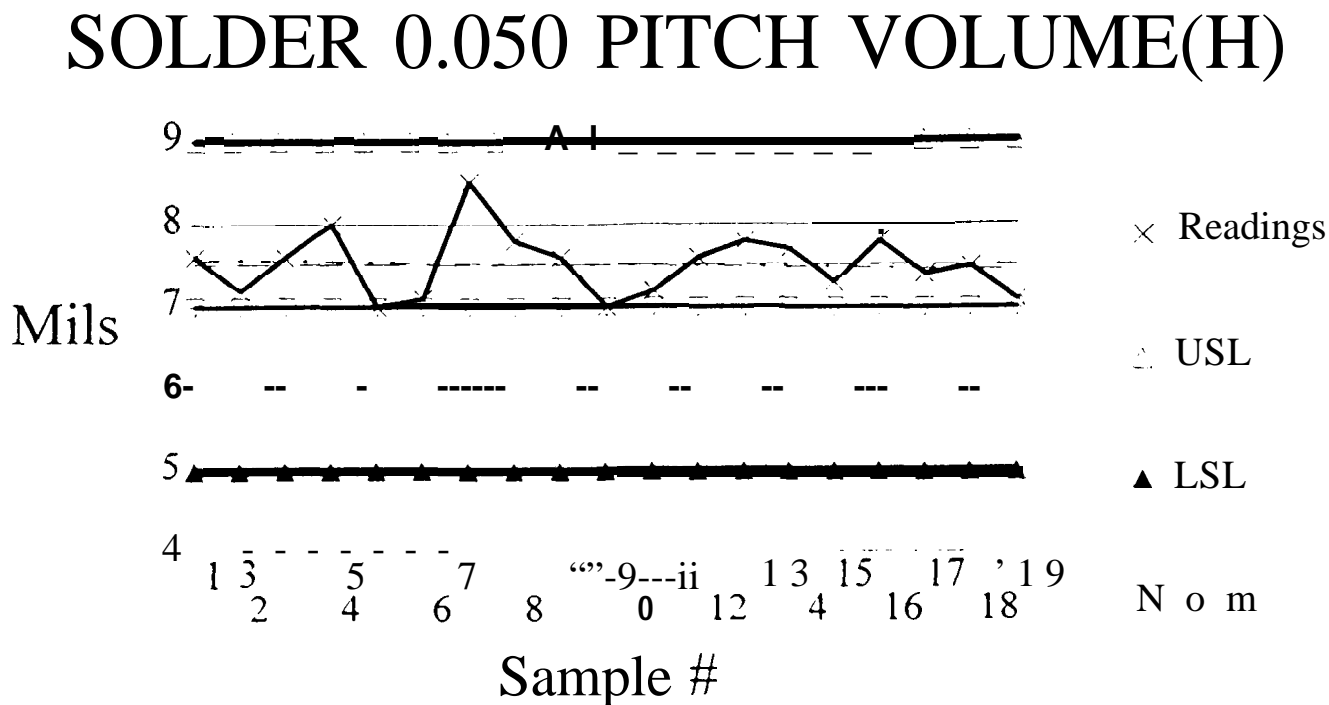


Figure:11

SOLDER 0.050 PITCH

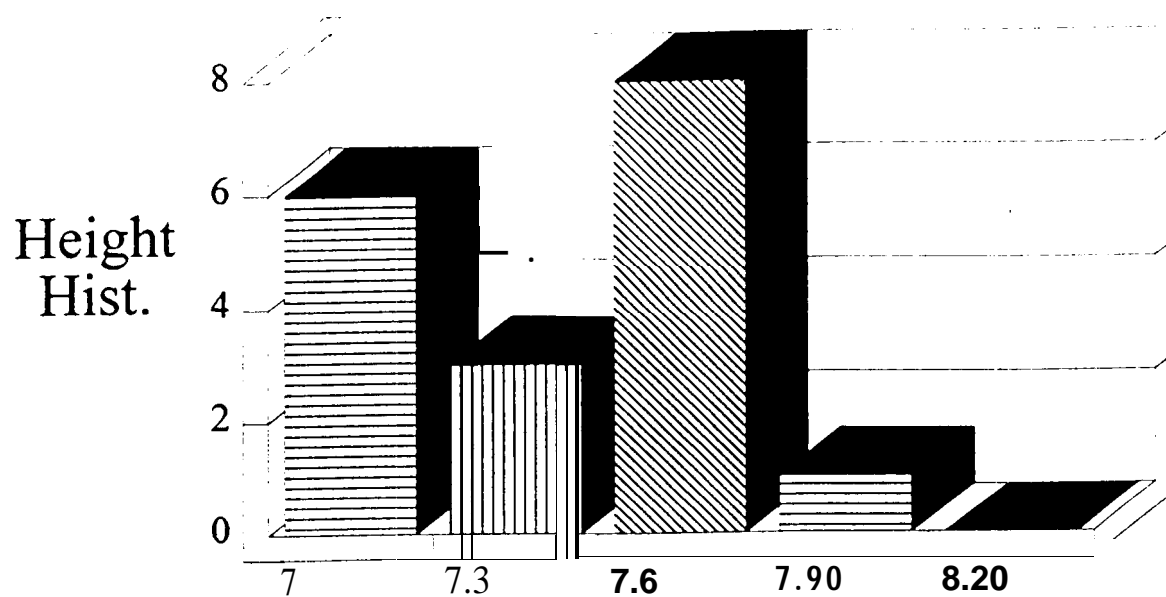


Figure: 12

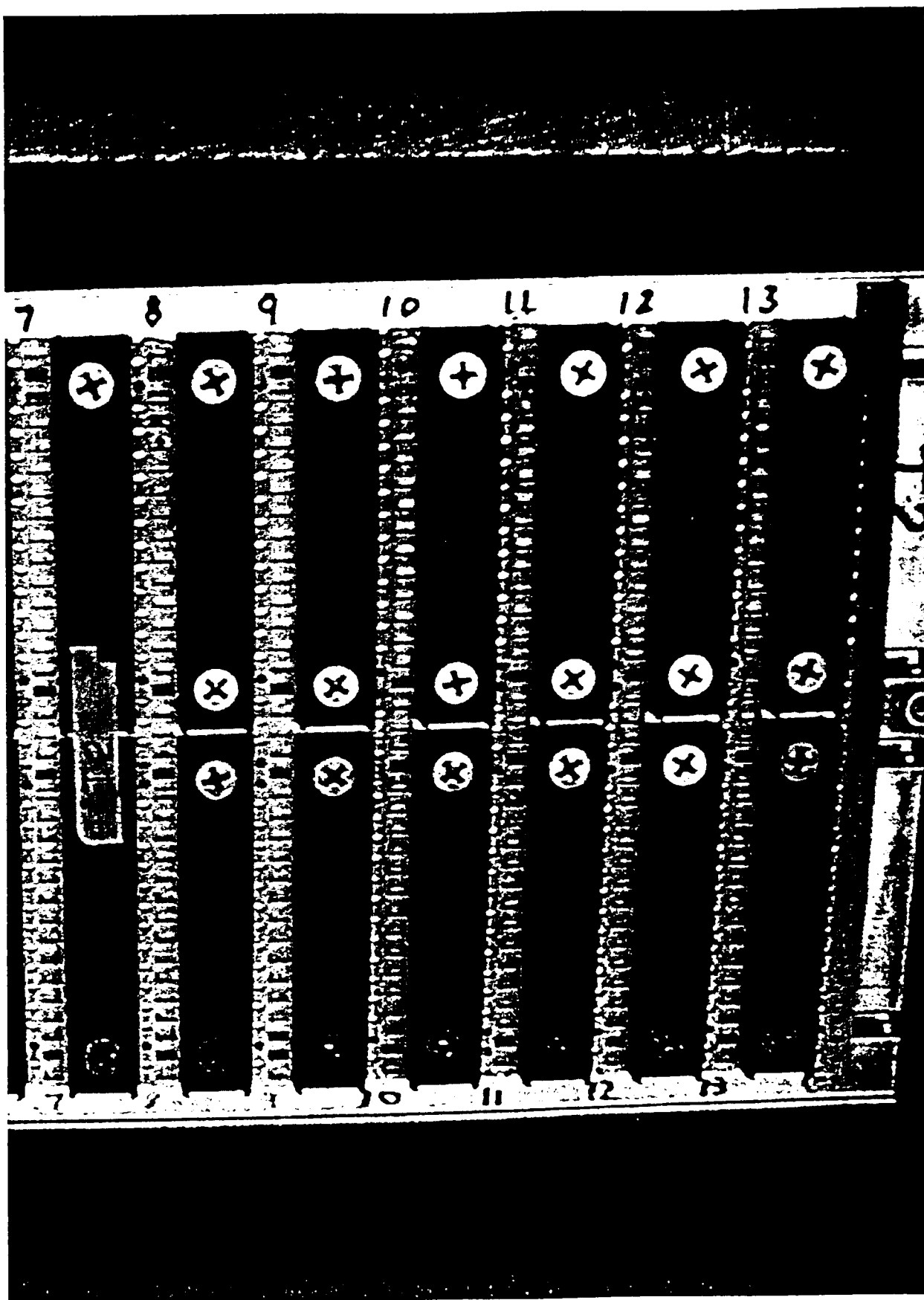


Figure: 13

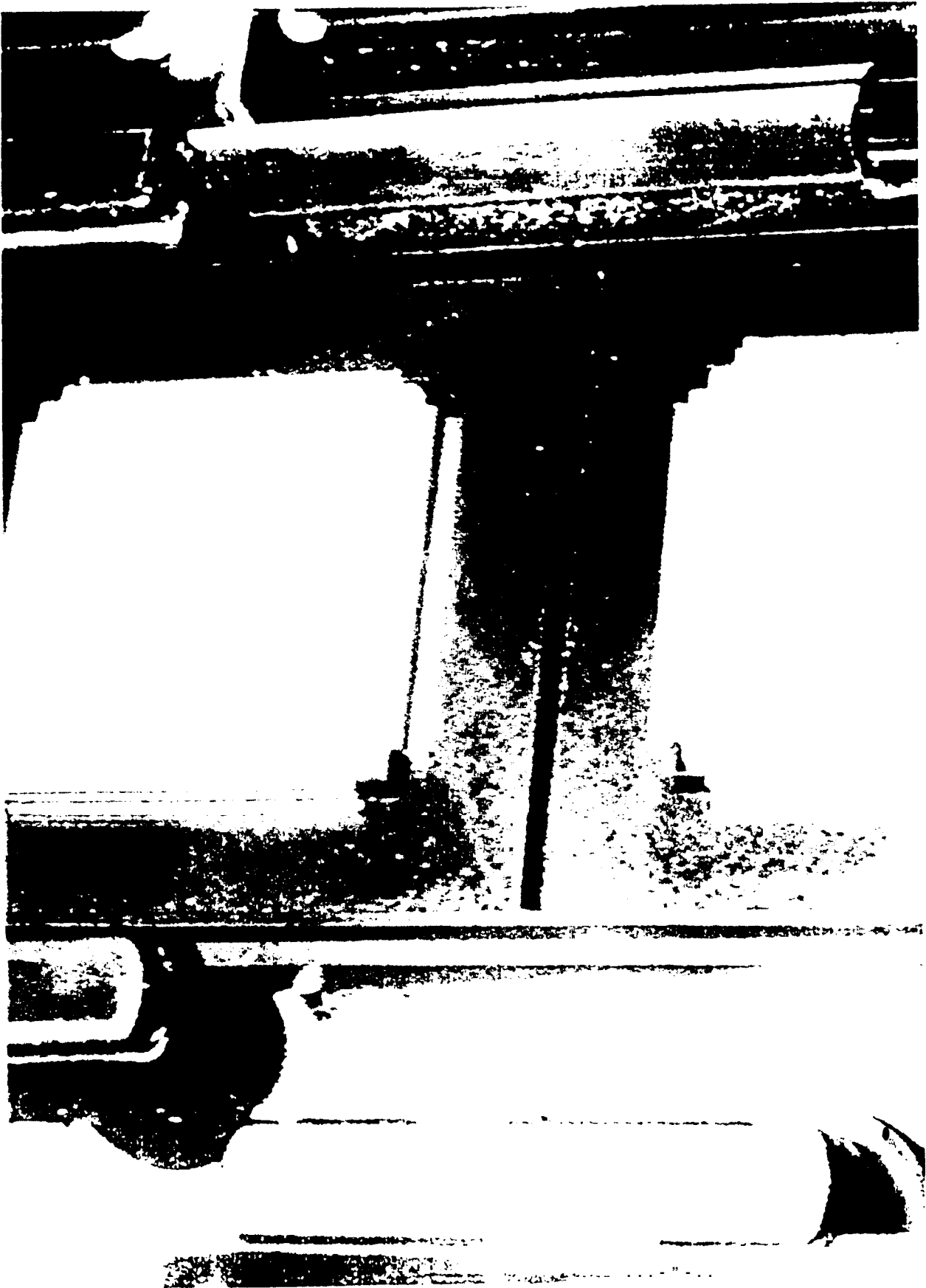
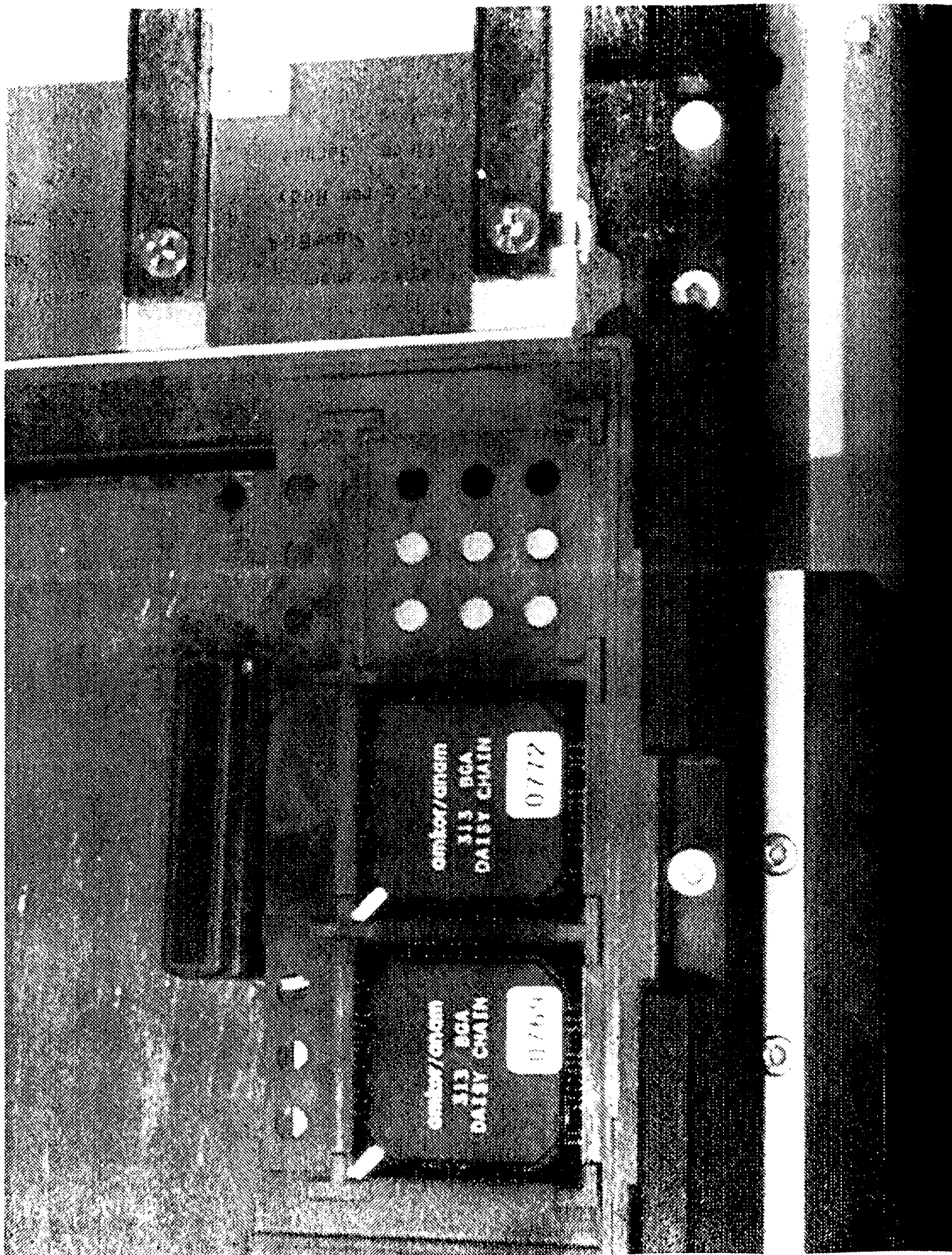


Figure 14



TOOLING PLATE INFORMATION

PCB 9612571A

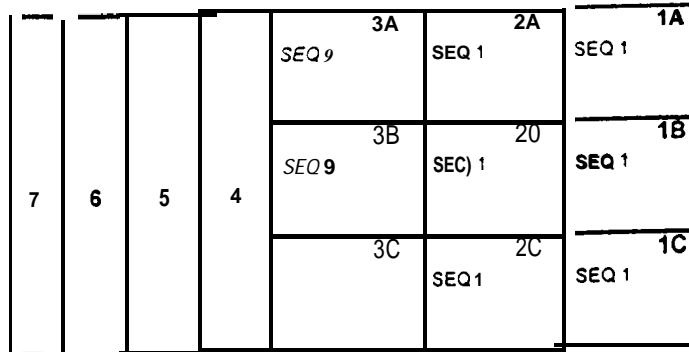
LAYOUT: HEMT PS REG. REVA

DATE: 10-20-97

REV. _A_

f-4

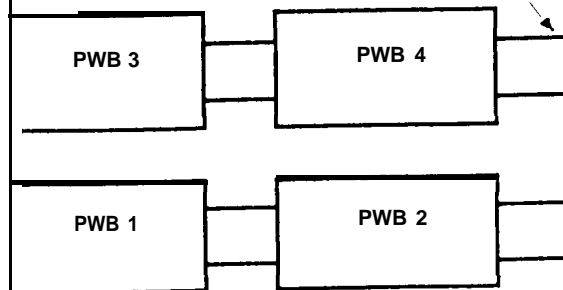
1	EQ 12	50
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NOTE
POLARITY FACING LEFT
OR BACK.

T-4 TRAY DIAGRAM

GOLD FINGERS



FRONT OF "Y" WAGON"

2 3 4 5 6 7 8 9 10 11:

RAY
T 7

SEC)	TOOL	LOC ON YW	WAF. TRAY #	PART NUMBER	PACKAGE	QTY.	COMMENTS
1	A14	T4_1A-1C	I-120-200265A-C	OP113ES	S08	2	U2, U4
		T4_2A-2C	H20_200265D-F	"			
2	A14	V188_SLOT 22	N/A	OP413ES	S016	4	U1, 3, 5, 6
3	A12	T7_ 1 & 2	N/A	CRCW06031003F	RC0603	5	R8, 10, 12, 20, 22, 24 100K
4	A12	T7_ 3 & 4	N/A	CRCW0603515J		6	R30, 32, 34 36, 38, 40 5.1 MEG
5	A12	T7_ 5, 11, 12	N/A	CRCW060310ROF		a	R1-R3 R6 R13-R15, R18 10 OHM
6	A12	T7_ 8, 9, 10	N/A	CRCW060310O2F		13	R7, R9, R19, R21, R27, R28, R29, R31, R33, R35, R37, R39, R41 10K
7	A12	T7_ 6	N/A	CRCW06031000F		1	R25 100 OHM
8	A12	T7_ 7	N/A	CRCW0603752J		1	R25 7.5K
9	A12	T4_ 1A, 1B	H20_120_24 24A	MGSF1N03LT1	SOT23	1	Q1
10	A12	TAPE REEL_1A	N/A	MMSZ4630T1	D1406	2	D9 D27 (2 pin SOIC form)
11	A12	TAPE REEL_15	N/A	MBR0520LT1		34	D1-D8 D10 - D26 D28-D36
12	A14	Y_4	N/A	293D476X0016D2T	CWR 110	2	C1, C2 47 uF
13	A13	TAPE REEL_12	N/A	VJ1210X474KXXMB	CC1210	3	C3 - C3 47 uF

Atul Menta

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11/18/97

Figure: 16



Figure: 17

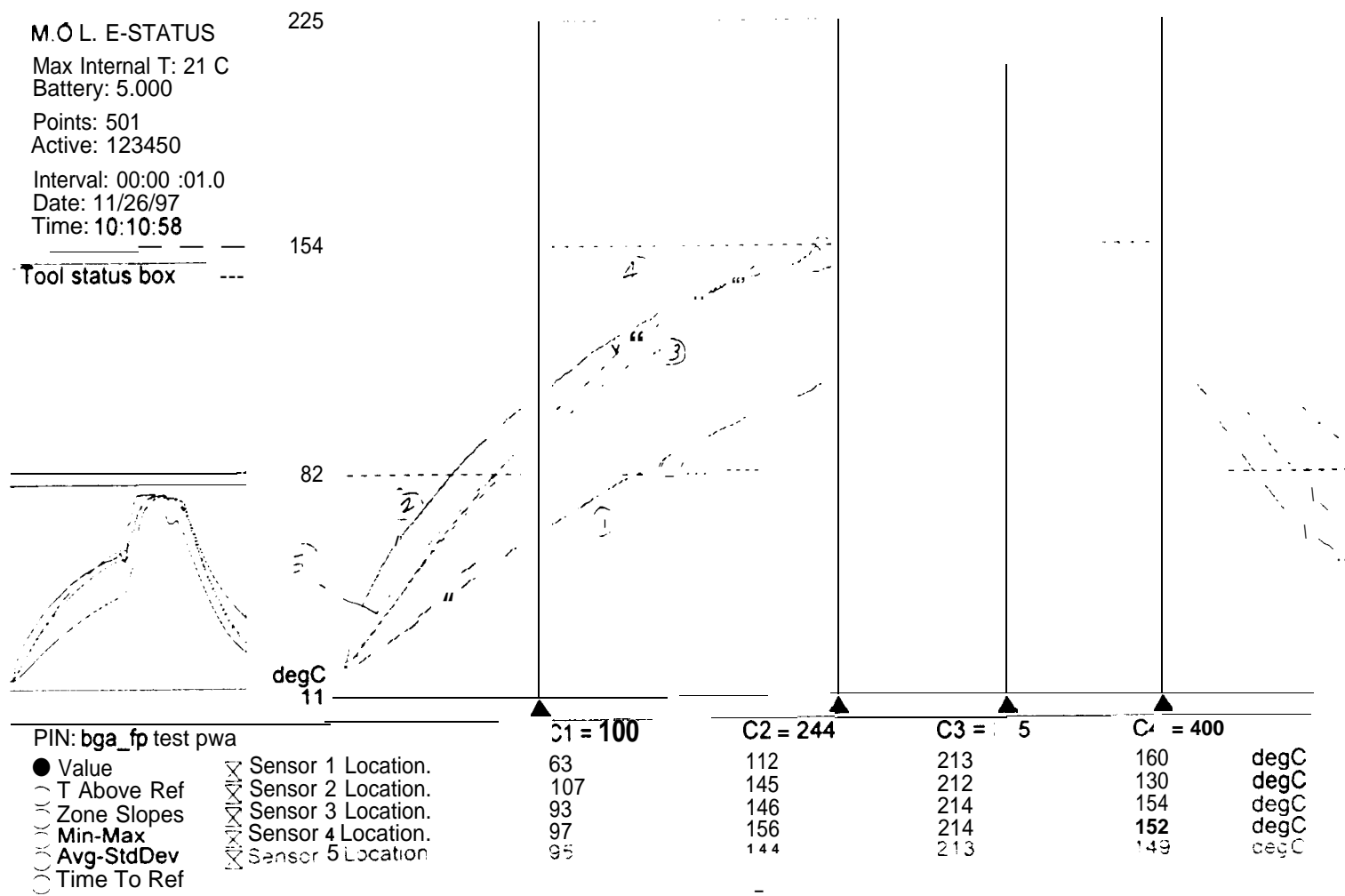


Figure: 18

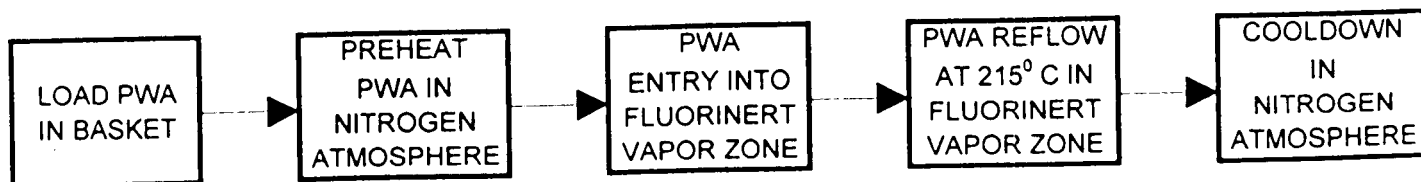


FIGURE 19

Airvac

Program Identification:

REM QFP132

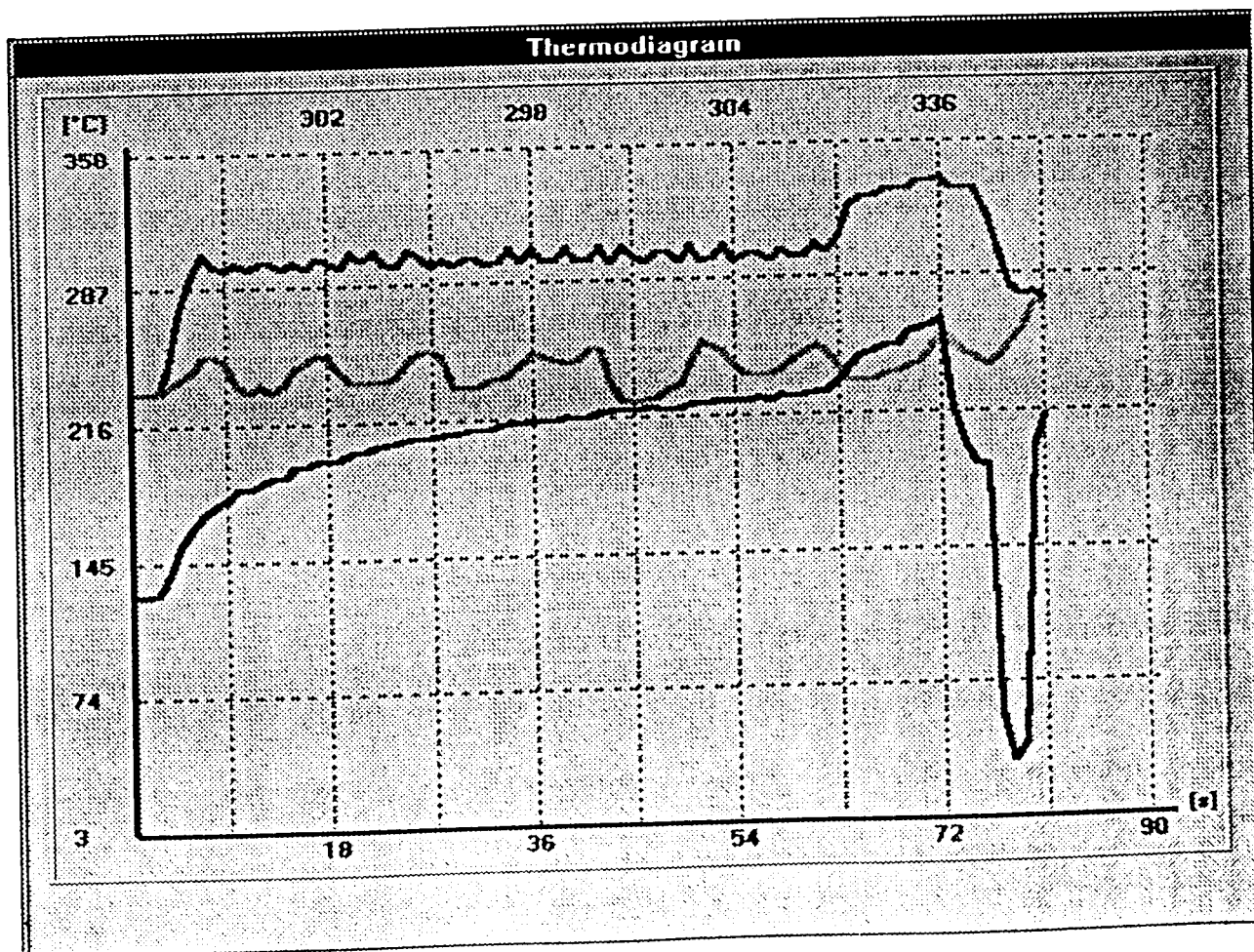
Name of Component: QFP 132, 33x33
PWB Identification: TEST BD
Operator: ATUL MEHTA
Actual Time: 15:36

Preheating
Temperature: 250°
Flow: 60"/0

Heating1
Temperature: 300°
Time: 60s
Flow: 70%

Heating2
Temperature: 340°
Time: 30s
Flow: 90%

Actual units are Celsius



Program Identification

PBGA-256

Name of Component

BALL GRID ARRAY

PWB Identification

Operator

ATUL MEHTA

Actual Time

14:44

Preheating

Temperature:

200°

Flow:

50%

Heating1

Temperature:

250°

Time:

100s

Flow:

600/0

Heating2

Temperature:

330°

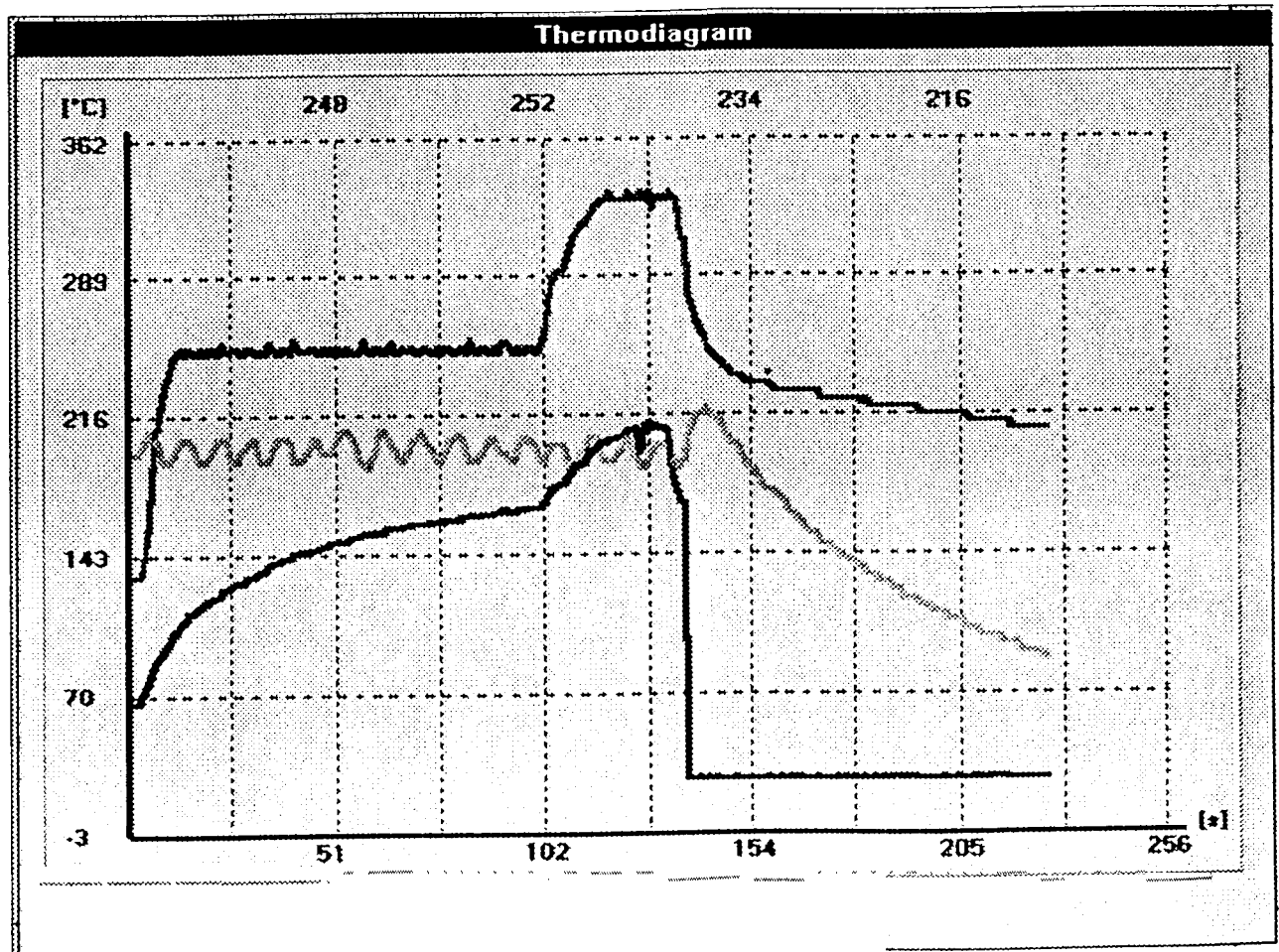
Time:

30s

Flow:

70%

Actual Units are Celsius



Program Identification

CBGA121

Name of Component PERI. BGA,CERAMIC
PWB Identification
Operator ATUL MEHTA
Actual Time 12:17

Preheating

Temperature. 200°
Flow: 600/0

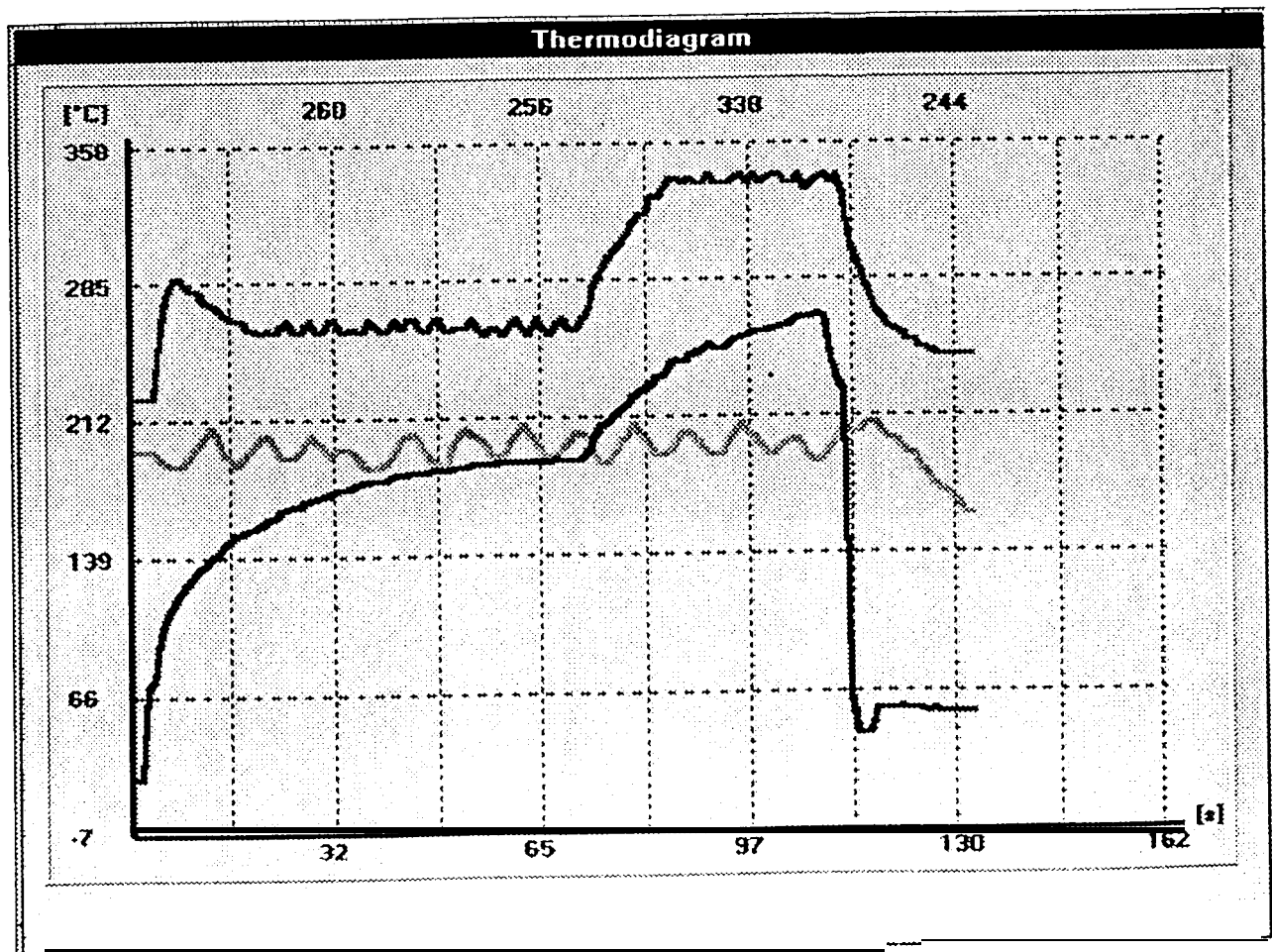
Heating1

Temperature: 260°
Time: 70s
Flow: 60%

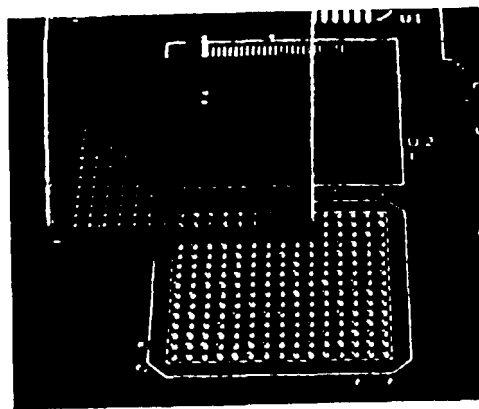
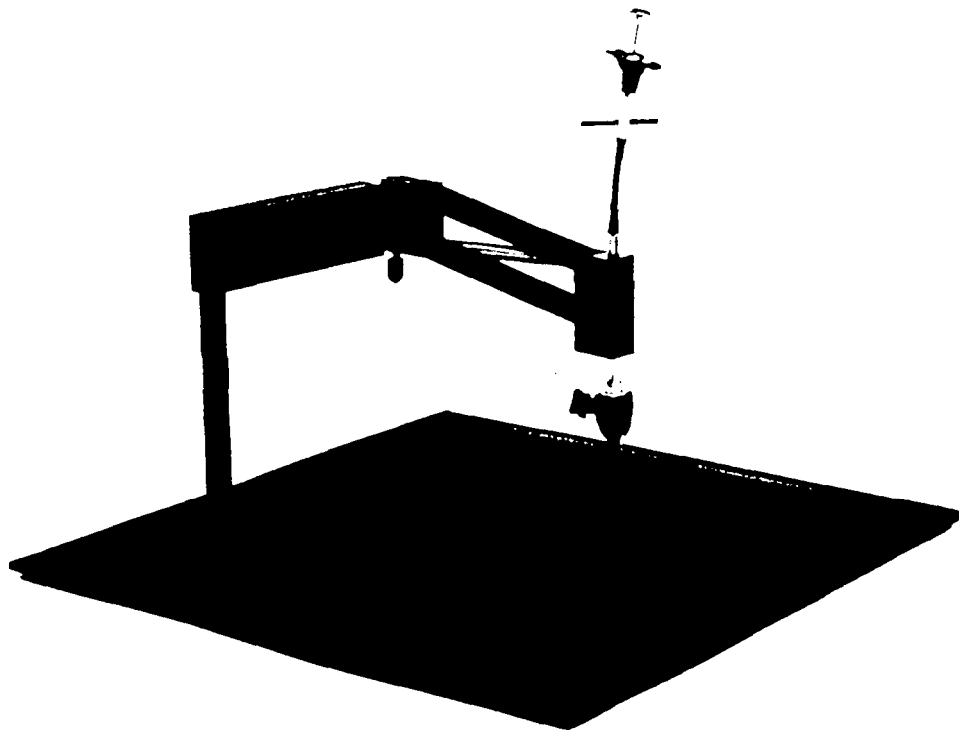
Heating2

Temperature: 340°
Time: 40s
Flow: 800/0

Actual units are Celsius



CONTINUOUS PROCESS IMPROVEMENT



BGA Solder print from precision stencil

FIGURE 23